Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-4 (Cancelled)

5. (Currently Amended) [[The]] A semiconductor device comprising: ~~as set forth in Claim 1,~~

a semiconductor substrate; and

a dielectric film including a porous film and a non-porous film in contact therewith formed on said semiconductor substrate,

wherein said porous film and said non-porous film are substantially of an identical composition,

[[said]] pores are distributed in a relatively lower density in the proximity of an upper surface of said dielectric film, and

the dielectric film includes an area where the density of said pores varies gradually toward the upper surface of said dielectric film.

6. (Currently Amended) A semiconductor device comprising: ~~as set forth in Claim 1,~~

a semiconductor substrate; and

a dielectric film including a porous film and a non-porous film in contact therewith formed on said semiconductor substrate,

wherein said porous film and said non-porous film are substantially of an identical composition, and

a metal interconnect is provided in said dielectric film, such that an upper surface of said metal interconnect and that of said dielectric film are aligned in [[a]] the same plane ~~plain~~.

Claims 7-10 (Cancelled)

11. (Currently Amended) [[The]] A semiconductor device comprising ~~as set forth in Claim 7,~~

a semiconductor substrate; and

a dielectric film including a porous film and a non-porous film in contact therewith formed on said semiconductor substrate,

wherein said porous film and said non-porous film both contain Si, O and C,

[[said]] pores are distributed in a relatively lower density in the proximity of an upper surface of said dielectric film, and

the dielectric film includes an area where the density of said pores varies gradually toward the upper surface of said dielectric film.

12. (Currently Amended) [[The]] A semiconductor device comprising ~~as set forth in Claim 7,~~

a semiconductor substrate; and

a dielectric film including a porous film and a non-porous film in contact therewith formed on said semiconductor substrate,

wherein said porous film and said non-porous film both contain Si, O and C, and

a metal interconnect is provided in said dielectric film, such that an upper surface of said metal interconnect and that of said dielectric film are aligned in [[a]] the same plane ~~plain~~.

13. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate; and

a dielectric film having a substantially uniform composition including a porous portion;

wherein pores in said porous portion are distributed in a relatively lower density either in the proximity of an upper surface or in the proximity of a lower surface of said dielectric film, and

the dielectric film includes an area where density of said pores varies gradually toward the upper surface or the lower surface of said dielectric film.

14. (Original) The semiconductor device as set forth in Claim 13, wherein said pores are distributed in a relatively lower density in the proximity of an upper surface of said dielectric film.

15. (Currently Amended) The semiconductor device as set forth in any of Claim 13, wherein a metal interconnect is provided in said dielectric film, such that an upper surface of said metal interconnect and that of said dielectric film are aligned in [[a]] the same plane ~~plain~~.

16. (Withdrawn) A method of manufacturing a semiconductor device comprising:

forming a dielectric layer on a semiconductor substrate by forming a porous film and forming thereon a non-porous film having a substantially same composition as said porous film;

selectively removing a portion of said dielectric film to form a recess;

forming a metal layer so as to fill said recess; and

performing either polishing or etch-back of said metal layer to an extent that said porous film is not exposed, to remove said metal layer formed outside said recess.

17. (Withdrawn) The method as set forth in Claim 16, wherein said forming said dielectric film includes forming said dielectric film in an integrated process without taking said substrate out of a CVD deposition chamber; and employing a deposition gas containing a template during a process of forming a porous portion of said dielectric film and employing a deposition gas not substantially containing a template during a process of forming a non-porous portion of the same.

18. (Withdrawn) A method of manufacturing a semiconductor device comprising:

forming a dielectric layer on a semiconductor substrate by forming a porous film containing Si, O and C and forming thereon a non-porous film containing Si, O and C;

selectively removing a portion of said dielectric film to form a recess;

forming a metal layer so as to fill said recess; and

performing either polishing or etch-back of said metal layer to an extent that said porous film is not exposed, to remove said metal layer formed outside said recess.

19. (Withdrawn) The method as set forth in Claim 18, wherein said forming said dielectric film includes forming said dielectric film in an integrated process without taking said substrate out of a CVD deposition chamber; and employing a deposition gas containing a template during a process of forming a porous portion of said dielectric film and employing a deposition gas not substantially containing a template during a process of forming a non-porous portion of the same.

20. (Withdrawn) A method of manufacturing a semiconductor device comprising forming a porous-structured dielectric film having a substantially uniform composition on a semiconductor substrate; wherein said forming said dielectric film includes controlling a deposition condition to vary a density of pores.

21. (Withdrawn) The method as set forth in Claims 20, wherein said forming said dielectric film includes performing CVD process and changing a deposition gas to vary a density of pores.

22. (Withdrawn) The method as set forth in Claim 20, wherein said forming said dielectric film includes controlling a deposition condition such that said pores are distributed in a relatively lower density in the proximity of an upper surface of said dielectric film.

23. (Withdrawn) The method as set forth in Claim 20, wherein said forming said dielectric film includes forming said dielectric film in an integrated process without taking said substrate out of a CVD deposition chamber; and employing a deposition gas containing a

template during a process of forming a porous portion of said dielectric film and employing a deposition gas not substantially containing a template during a process of forming a non-porous portion of the same.

24. (Withdrawn) A method of manufacturing a semiconductor device comprising:

forming a dielectric film on a semiconductor substrate by forming a first film containing a template and forming a second film not containing a template in this sequence;

selectively removing a portion of said dielectric film to form a recess; and

performing heat treatment on said first film to decompose or remove said template, thereby forming a porous structure in said dielectric film.

25. (Withdrawn) The method as set forth in Claim 24, further comprising:

forming a metal layer so as to fill said recess; and

performing either polishing or etch-back of said metal layer until a surface of said dielectric film is exposed, to remove said metal layer formed outside said recess.

26. (Withdrawn) The method as set forth in Claim 24, wherein said forming said dielectric film includes forming said dielectric film in an integrated process without taking said substrate out of a CVD deposition chamber; and employing a deposition gas containing a template during a process of forming a porous portion of said dielectric film and employing a deposition gas not substantially containing a template during a process of forming a non-porous portion of the same.

27. (New) The semiconductor device as set forth in claim 6, wherein the metal interconnect is a damascene interconnect line.

28. (New) The semiconductor device as set forth in claim 12, wherein the metal interconnect is a damascene interconnect line.